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Comparative Analysis of DE–HHO Optimized PD/APOD-PWM for a 15-Level Asymmetric Multilevel Inverter

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Abstract

In this paper, a single-phase 10-switch three isolated DC sources (10 V: 20 V: 40 V) based 15-level asymmetric multilevel inverter is presented. A complete analysis of all the 1024 gate combinations verifies all the 15 output levels and 1 switching state for each non-zero level, as well as the full set of forbidden states. Four operating modes (DE-PD, DE-APOD, HHO-PD and HHO-APOD) are simulated with an identical objective, constraints, evaluation budget and 7 quarter -wave switching angles optimized using Differential Evolution (DE) and Harris Hawks Optimization (HHO). The angle sets generated by the two optimizers were very similar (maximum difference of 1.14°). For both PD modes, the voltage THD was 6.957% and the current THD was 0.127%, respectively, while for both APOD modes, these parameters were, respectively, 6.679% and 0.116%. Both modes of the APOD saw a 4.0% and 8.7% reduction in the voltage THD and current THD, respectively, while the choice of optimizer did not measurably affect the simulated output.

Keywords: 15-Level Inverter, Asymmetric Multilevel Inverter, Reduced Switch Count, Switching-Angle Optimization, Differential Evolution, Harris Hawks Optimization, Level-Shifted PWM, PD, APOD, Total Harmonic Distortion.

1. Introduction

Multilevel inverters (MLIs) generate an approximated staircase sinusoid using multiple DC voltages. This has lowered the voltage stress on the devices, has lowered the dv/dt and the harmonic distortion [1], [2] and MLIs are widely used in medium-voltage drives and grid-connected power conversion [3]. As the number of levels of the classical topologies grows, they require an increasing number of switches, gate drivers and passive components, and this has stimulated the study of reduced-switch-count (RSC) topologies [4]–[6]. Three DC sources supply $2^3 = 8$ non-negative levels with an asymmetric binary source ratio, and in combination with a polarity-reversal stage, 15 output levels [4], [7].

In this topology (Fig. 1), the number of switches is 10, as it includes 3 series-connected cells, with 2 switches in each cell and an H-bridge. The topology itself is not claimed as new. The study involves its modulation, such as optimal switching angles selection and the arrangement of the carrier of the

level-shifted PWM on the same circuit and load, and examines the influence of these arrangements on the output quality.

One of the methods called selective harmonic elimination (SHE) is designed to calculate the staircase switching angles in advance to ensure that the amplitude of the fundamental is achieved as a prescribed value while the low order harmonics are minimized [8], [9]. These equations are non-linear and transcendental, so that they are normally solved by metaheuristic optimizers [10] and [11]. Multicarrier level-shifted PWM (LS-PWM) uses a sinusoidal reference and a stack of triangular carriers whose performance is dependent on the carrier disposition, e.g., phase disposition (PD) or alternative phase-opposition disposition (APOD) [12], [13].

This paper is an extension of the authors' previous research on an 11 level MLI optimized using a Genetic Algorithm and Particle Swarm Optimization. In the present study, it is used a different topology with two different optimizers Differential Evolution (DE) [14], [15] and Harris Hawks Optimization (HHO) [16] as well as new MATLAB/Simulink results. The contributions are:

- Ten-switch 15-level topology with switching-state analysis (verified by a complete enumeration of all 1024 gate combinations).
- Solved with DE and HHO under the same conditions with a 7 angle formulation, developed from the binary level transitions.
- A MATLAB/Simulink comparison between four modes (DE-PD, DE-APOD, HHO-PD, HHO-APOD) which involves separating the effect of the optimizer from that of the disposition of the carrier.

2. Literature Review

2.1 Reduced-Switch 15-Level Topologies:

The reduced-switch-count MLIs have been reviewed in terms of the number of devices, the number of isolated source devices, the blocking voltage, and the necessity of a polarity generation stage [4–6] and Babaei's cascaded sub-multilevel structure is a previous version of series cells followed by polarity reversal [7]. Recent 15 level designs include a 12-4 topology with nearest level control [17], 10-4 topology with lower total standing voltage (TSV) [18], asymmetric topology without an H-bridge [19] and reduced component topology with PSO computed angles [20] at 15 and 25 levels. These works report that the full peak voltage needs to be blocked by the back-end H-bridge, increasing the TSV [20], [21]. It can be done using 15 levels of 10 switches (ten H-bridge switches) and only 3 sources, but the H-bridge switches have to block $7V_{dc}$.

2.2 Switching-Angle Optimization and Multicarrier PWM:

SHE solutions are only possible if the modulation index and the set of selected harmonics are appropriate. [8]; and when they do not exist, algebraic methods will yield all solutions but their

performance is poor when the number of angles increases [9], unequal DC levels will necessitate step-weighted Fourier coefficients [10], and selective harmonic mitigation (SHM) solutions will bound the harmonics rather than eliminate them [22], [23]. DE has been used in SHE in a nine level inverter with experimental verification [24] and hybridized with Broyden's method for a seven level cascaded H-bridge [25] and hybridized with grey wolf optimization [26]. In [16] the HHO technique has been used in a 9 -level modular inverter and contrasted with PSO and ant -colony optimization [27]. The main other alternative is carrier -based level -shifted PWM [12] which produces different distributions of the carrier and sideband harmonics as determined by the PD, POD and APOD dispositions, and the differences are directly reflected in the output voltage in single -phase operation.

2.3 Research Gap:

Most of the published results for the ten-switch binary 15 -level topology employ nearest-level control or a single optimizer, while comparative optimization studies do not often also balance the evaluation budget and the objective between the algorithms, but this is required for a fair ranking [28], [29]. There is no controlled comparison to determine the effect of each factor separately in which two optimizers and two carrier dispositions are used together on the same circuit and load. The comparison is presented in this paper in MATLAB/Simulink. None of the DE, HHO or topology is claimed as being novel.

3. Proposed 15-Level Asymmetric Inverter Topology

3.1 Circuit Description:

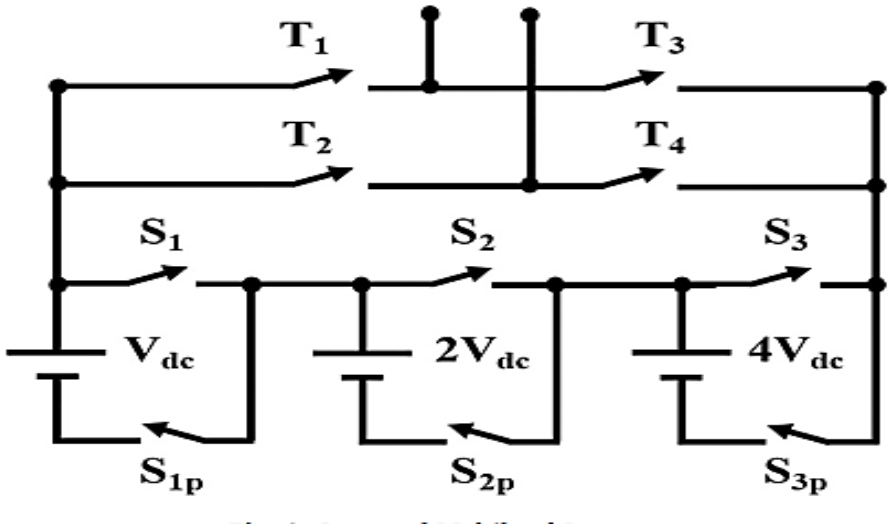

Fig. (1): Proposed 15-level asymmetric multilevel inverter: three series cells (V_{dc}, $2V_{dc}$, $4V_{dc}$) with bypass switches S_1–S_3 and insertion switches S_{1p}–S_{3p}, and an H-bridge T_1–T_4.

The circuit is shown in Fig. 1. The left rail P is the positive rail of the V_{dc} source, the right rail N is the common node of S_3, S_{3p}, T_3 and T_4. The internal nodes N_1 and N_2 are connected to S_1–S_2 and S_2–S_3, respectively, and are also the positive terminals of the $2V_{dc}$ and $4V_{dc}$ sources. The negative terminal of source i is connected to the next node by each insertion switch S_{ip}, therefore a cell offers two connections between their input and output terminals: the bypass switch S_i (0 V) or the source in series with S_{ip} ($+V_i$). A and B are the middle points of H-bridge legs T_1/T_3 and T_2/T_4. If the insertion variables are binary, then:

$$v_{PN} = V_{dc}(s_{1p} + 2s_{2p} + 4s_{3p}), \quad s_i = 1 - s_{ip} \qquad (1)$$

$$v_{AB} = (T_1T_4 - T_2T_3) \cdot v_{PN} \qquad (2)$$

Because the cell code (s_{1p}, s_{2p}, s_{3p}) is the binary representation of the level index k = 0…7, the circuit produces $2 \cdot 2^3 - 1 = 15$ levels, the H-bridge reversing the polarity. Table 1 summarizes the main parameters of the inverter and of the simulation.

Table (1): System, PWM and simulation parameters

Parameter	Value
DC sources (isolated)	V_{dc} = 10 V, $2V_{dc}$ = 20 V, $4V_{dc}$ = 40 V (ideal DC voltage sources in Simulink)
Output levels	15 (0, ±10 V … ±70 V); $V_{max} = 7V_{dc}$ = 70 V
Switches / gate drivers	10 IGBT / 10 gate drivers
Blocking voltage per device	S_1, S_{1p}: V_{dc}; S_2, S_{2p}: $2V_{dc}$; S_3, S_{3p}: $4V_{dc}$; T_1–T_4: $7V_{dc}$
Total standing voltage (TSV)	$42V_{dc}$ = 420 V (TSV_{pu} = 6); no redundant states for non-zero levels
Fundamental frequency / modulation index	50 Hz / M = 1.0 (V_1 = 70 V peak)
Load	series RL: R = 10 Ω, L = mH 70 (|Z| ≈ 24 Ω at 50 Hz from V_1 = 70 V and $I_1 \approx 2.9$ A)
PWM carriers	7 level-shifted carriers, PD or APOD, rectified reference; f_c = 3300Hz
Operating modes	Mode 1 DE-PD, Mode 2 DE-APOD, Mode 3 HHO-PD, Mode 4 HHO-APOD
Simulation / FFT	Discrete, fixed step 1×10^{-5} s (powergui)

3.2 Switching States:

Ideal switches and sources have been used to test all $2^{10} = 1024$ gate combinations in the circuit net list. If a source has both terminals in the same connected set of nodes, it is a short circuit; if the output terminals are not connected by any potential, it is an open circuit; otherwise, it is valid. The enumeration gave 170 valid, 637 short-circuit and 217 open states. The output voltage that the valid states generate is only 15 different voltages, ranging from $-7V_{dc}$ … $+7V_{dc}$. Each cell and each H-bridge leg has two allowed switching states, with complementary operation, which results in each non-zero level having exactly one switching state. Each short-circuit state activates both (S_i, S_{ip}), (T_1, T_3) or (T_2, T_4) and switching both of any of these cells off breaks the series path. Therefore, complementary switching with dead time is necessary. The switching states are given in Table 2.

Table (2): Switching states of the 15-level inverter (1 = ON). The cell code (S_{1p} S_{2p} S_{3p}) is the binary level index. Negative levels $-kV_{dc}$ use the same cell codes with T_2 and T_3 ON

v_{AB}	T_1 T_2 T_3 T_4	S_1 S_2 S_3	S_{1p} S_{2p} S_{3p}	Conduction path / sources in circuit	Status
$+7V_{dc}$ (+70 V)	1 0 0 1	0 0 0	1 1 1	T_1→load→T_4; sources: $4V_{dc}$ + $2V_{dc}$ + V_{dc}	Valid
$+6V_{dc}$ (+60 V)	1 0 0 1	1 0 0	0 1 1	T_1→load→T_4; sources: $4V_{dc}$ + $2V_{dc}$	Valid
$+5V_{dc}$ (+50 V)	1 0 0 1	0 1 0	1 0 1	T_1→load→T_4; sources: $4V_{dc}$ + V_{dc}	Valid
$+4V_{dc}$ (+40 V)	1 0 0 1	1 1 0	0 0 1	T_1→load→T_4; sources: $4V_{dc}$	Valid
$+3V_{dc}$ (+30 V)	1 0 0 1	0 0 1	1 1 0	T_1→load→T_4; sources: $2V_{dc}$ + V_{dc}	Valid
$+2V_{dc}$ (+20 V)	1 0 0 1	1 0 1	0 1 0	T_1→load→T_4; sources: $2V_{dc}$	Valid
$+1V_{dc}$ (+10 V)	1 0 0 1	0 1 1	1 0 0	T_1→load→T_4; sources: V_{dc}	Valid
0	1 0 0 1 or 0 1 1 0	1 1 1	0 0 0	All cells bypassed (S_1–S_2–S_3); used at half-cycle boundaries	Valid
—	T_1&T_3 or T_2&T_4 = 1	—	—	Shoot-through of an H-bridge leg	Forbidden
—	—	$S_i = S_{ip} = 1$		Short circuit of source i	Forbidden
—	—	$S_i = S_{ip} = 0$		Series path open (diode freewheeling)	Not allowed

In the Simulink model (Fig. 4), the blocks T3, T1, T4, T2 (gate signals [T1]–[T4]) are the H-bridge switches of Fig. 1, the insertion switches S_{1p}, S_{2p} and S_{3p} are the blocks T8, T9 and T10 (gate signals [s1]–[s3]), and the bypass switches S_1, S_2 and S_3 are the blocks T5, T6 and T7 (gate signals [s4]–[s6]).

3.3 Blocking Voltage and Switching Sequence:

The voltage blocked in each cell is its own voltage and each H-bridge switch blocks $7V_{dc}$, so that the total voltage blocked is $TSV = 2(1 + 2 + 4)V_{dc} + 4 \cdot 7V_{dc} = 42V_{dc}$.

This is the main cost of the H-bridge unfolding stage. The commutation is done only at zero voltage at the fundamental frequency, the zero level is obtained by bypassing all of the cells, thus the load current passing through the bypass switches. For a fundamental frequency staircase, the transitions 1 to 2, 3 to 4 and 5 to 6 involve two or three cells; the dead time for these transitions needs to be applied per cell. The 7 angles shown in Fig. 5 are quarter-wave symmetric with each level being entered twice: once on the rising and once on the falling part of the half cycle.

4. Switching-Angle Formulation

4.1 Fourier Model:

Let V_1, V_2, V_3 be the source voltages. Level k equals $b_0V_1 + b_1V_2 + b_2V_3$, where (b_0, b_1, b_2) are the binary digits of k, so the step at angle θ_k is $\Delta V_k = [V_1, V_2 - V_1, V_1, V_3 - V_1 - V_2, V_1, V_2 - V_1, V_1]_k$. The output is quarter-wave symmetric (QWS), which means:

$$v_{AB}(\omega t) = \Sigma_{n = 1, 3, 5, \ldots} V_n \sin(n\omega t), \quad V_n = (4 / n\pi) \Sigma_{k=1}^{7} \Delta V_k \cos(n\theta_k) \qquad (3)$$

For the exact ratio 1:2:4 all steps equal V_{dc} and (3) reduces to:

$$V_n = (4V_{dc} / n\pi) \Sigma_{k=1}^{7} \cos(n\theta_k), \text{ n odd} \qquad (4)$$

4.2 Modulation Index and Constraints:

The modulation index is defined relative to the peak available voltage,

$$M = V_1 / (7V_{dc}) \quad \Rightarrow \quad \Sigma_{k=1}^{7} \cos \theta_k = 7\pi M / 4 \qquad (5)$$

Its rated value is M = 1 which yields $V_{max} = 7V_{dc} = 70$ V, and all results are measured at this value. The angles must satisfy $\delta \le \theta_1 < \theta_2 < \ldots < \theta_7 \le \pi/2 - \delta$ with gaps of at least $\delta = 1°$, which leaves time for dead time and the minimum pulse width.

4.3 Objective Function:

In a single-phase inverter, the triplen harmonics are not eliminated by the phase connection and it is impossible to exactly eliminate the 3rd–13th harmonics with seven angles over most of the modulation range, so the angles are found using constrained minimization [22]. The THD is calculated up to 49th harmonic and is included in the result.

$$THD = \sqrt{(\Sigma_{n=3,5,\ldots,49} V_n^2)} / V_1 \qquad (6)$$

The objective minimized by both algorithms is:

$$F(\theta) = w_1 e_1^2 + w_3 THD^2 + \Pi(\theta), \quad w_1 = 100, \; w_3 = 1 \qquad (7)$$

In the above, $e_1 = (\Sigma \cos \theta_k - 7\pi M/4)/(7\pi M/4)$ is the normalized fundamental error, and $\Pi(\theta)$ is a quadratic penalty on violations of the minimum gap δ. The large weight on e_1 keeps the fundamental within about 0.1% of its target. The same objective, constraints and repair (clipping to [0, π/2] and sorting) are used by DE and HHO.

5. Differential Evolution and Harris Hawks Optimization

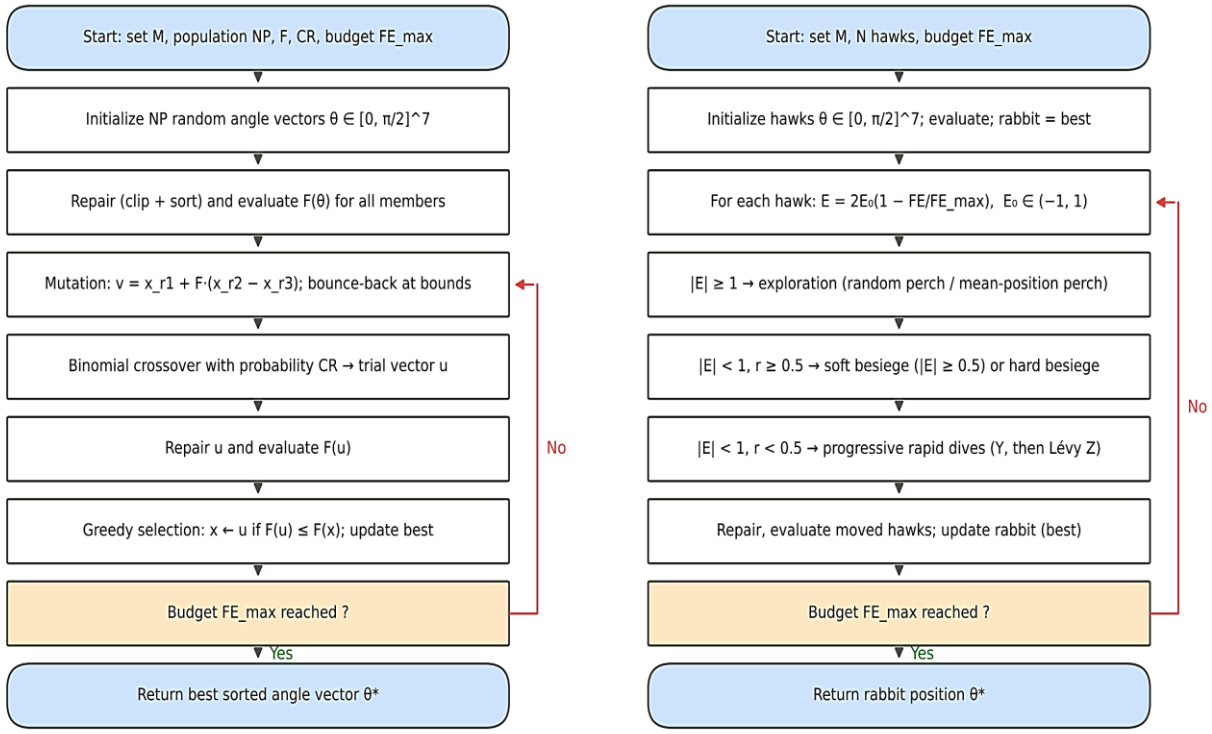

Fig. (2): Flowcharts of (a) the DE algorithm and (b) the HHO algorithm for switching-angle optimization

Each vector $x_i \in [0, \pi/2]^7$ is a possible angle vector in DE [14]. The population is randomly initialised, for every target vector a mutant is generated from three randomly selected population members (DE/rand/1) and a trial vector is created using binomial crossover:

$$v_i = x_{r1} + F\,(x_{r2} - x_{r3}) \tag{8}$$

$$u_{i,j} = v_{i,j} \text{ if } (r_j \le CR \text{ or } j = j_{rand}), \quad \text{otherwise } x_{i,j} \tag{9}$$

The better of target and trial is kept, which is the greedy selection algorithm. F scales the search step, and CR scales the number of angles inherited from the mutant, the components are reflected halfway towards the parent out of the bounds. In HHO [16], each hawk is considered as a candidate angle vector and the best solution is the rabbit. The escaping energy

$$E = 2E_0(1 - t/T), \quad E_0 \sim U(-1, 1) \tag{10}$$

Decreases over the run. When $|E| \geq 1$, the hawks wander up and down or around the mean hawk position and when $|E| < 1$ they exploit by soft or hard besiege around the rabbit or by progressive rapid dives with Lévy flights ($\beta = 1.5$) [16]. In this case, the fraction of the evaluation budget already expended is t/T (T being the total evaluation budget), and the evaluations of the dives are counted, thus allowing both algorithms to terminate at the same evaluation cost. The settings are given in Table 3 and the flowcharts in Fig. 2.

Table (3): Parameters of the DE and HHO optimizers

Parameter	DE	HHO
Search strategy	DE/rand/1/bin, greedy selection, bounce-back bounds	exploration, soft/hard besiege, rapid dives; $E = 2E_0(1 - FE/FE_{max})$
Population	NP = 40	N = 40
Control parameters	F = 0.5, CR = 0.9	Lévy exponent $\beta = 1.5$
Budget (function evaluations)	40 000	40 000
Independent runs	3 (best kept)	3 (best kept)
Objective, constraints, repair	Eqs. (6)–(7), clipping and sorting	identical to DE

6. Level-Shifted PWM and Operating Modes

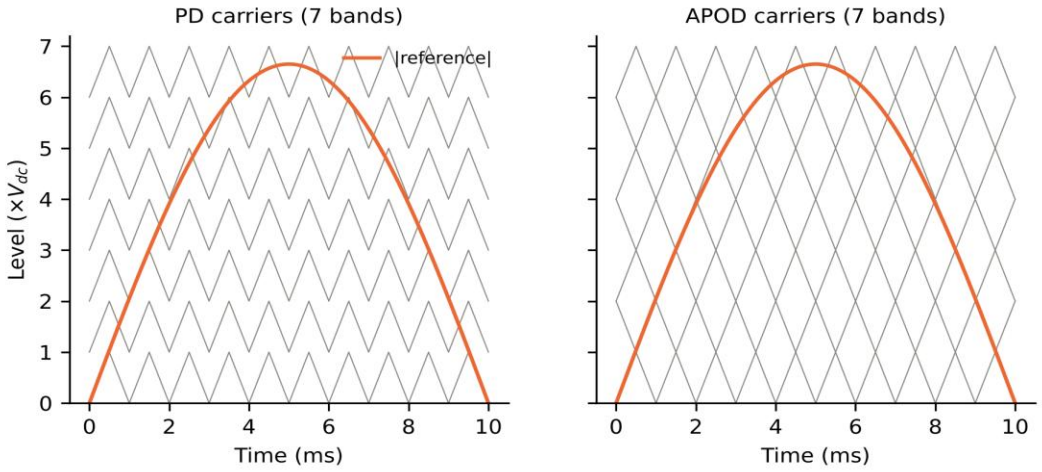

Fig. (3): Level-shifted carrier arrangements: phase disposition (PD, left) and alternative phase-opposition disposition (APOD, right), compared with the rectified reference (M = 0.95, f_c = 1 kHz shown for clarity)

The H-bridge gives the polarity and the inverter is modulated by seven carriers stacked in the band [0, 1] V_{dc}, [1, 2] V_{dc}, …, [6, 7] V_{dc} and compared to the rectified reference (Fig. 3):

$$r(t) = 7M\,|\sin(\omega t)|, \quad c_j(t) = (j - 1) + \mathrm{tri}(f_c t), \quad j = 1 \ldots 7 \qquad (11)$$

$$k(t) = \lfloor r(t) \rfloor + [\, r(t) - \lfloor r(t) \rfloor > \mathrm{tri}_j(t) \,] \qquad (12)$$

Where the tri(·) is a unit triangular carrier with frequency f_c and the k(t) is the level index applied to the cells by the binary coding of Table 2. In PD all the carriers are in phase, and in APOD the carriers

of neighbouring bands are in phase opposition [12], [13]. The two optimized angle sets are tested in the two carrier dispositions: Mode 1 DE-PD, Mode 2 DE-APOD, Mode 3 HHO-PD and Mode 4 HHO-APOD. Since the simulated output for modes 1 and 3 and for modes 2 and 4 are the same (Section 8.3), this paper does not claim an independent effect of the optimizer on the PWM output; it is rather considered as a comparison of the two carrier dispositions for each angle set.

7. MATLAB /Simulink Implementation and DC Sources

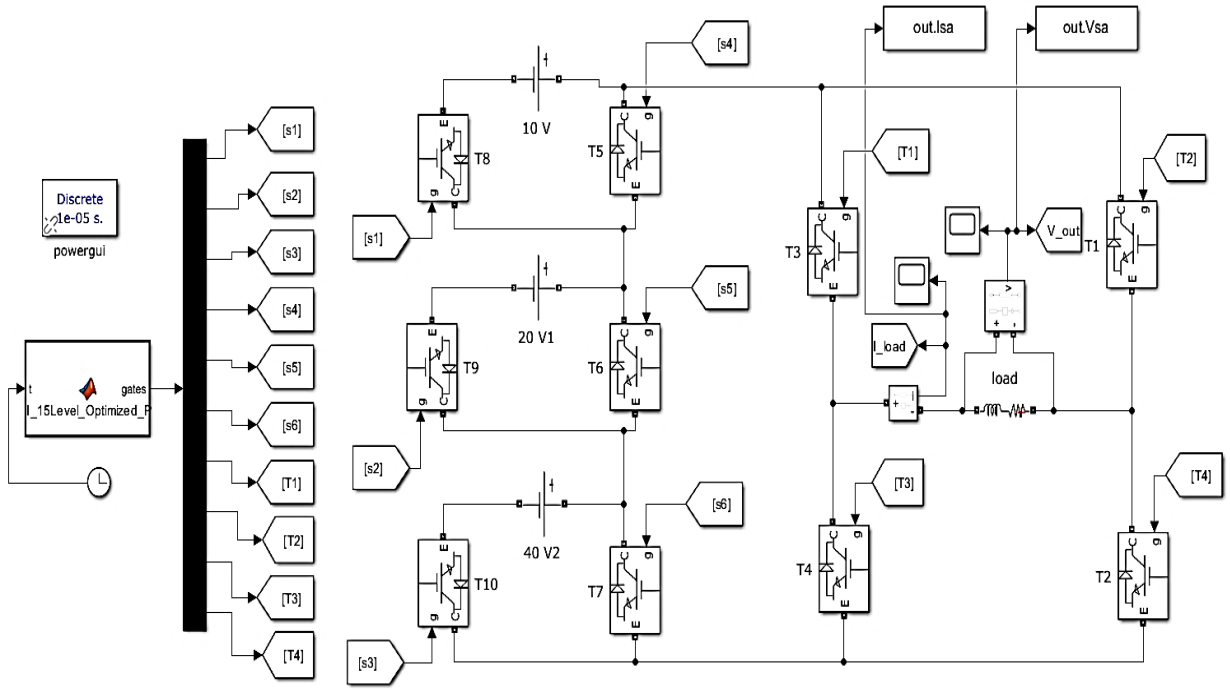

Fig. (4): MATLAB/Simulink model of the 15-level asymmetric inverter with the gate-pulse generator (MATLAB Function block), ten IGBT/diode switches, RL load and measurements

The circuit of Fig. 1 was built in MATLAB/Simulink (Specialized Power Systems) with three DC voltage sources of 10, 20 and 40 V, ten IGBT/diode blocks and a series RL load (Fig. 4). The ten gate signals for each mode are generated by a MATLAB Function block driven by the simulation clock that is binary coded as given in Table 2; the H-bridge commutates on the zero crossing of the reference. The FFT analysis of the output voltage and load current were performed in steady state, while the THD calculation was performed using the normalized harmonic spectrum. The parameters for the simulations are listed in Table 1, and the pulses to be inserted into the gates are displayed in Fig. 5.

They need to be galvanically isolated (separate batteries or separated DC supplies), as the negative terminals of the three sources are at different potentials and need to be rated individually, as the $4V_{dc}$

source provides the greatest proportion of the load power. They are ideal DC sources in the simulation, and the results can be used to characterize the inverter and its modulation when the source voltage is fixed, while deviations from source voltage and source impedance are not studied in this paper.

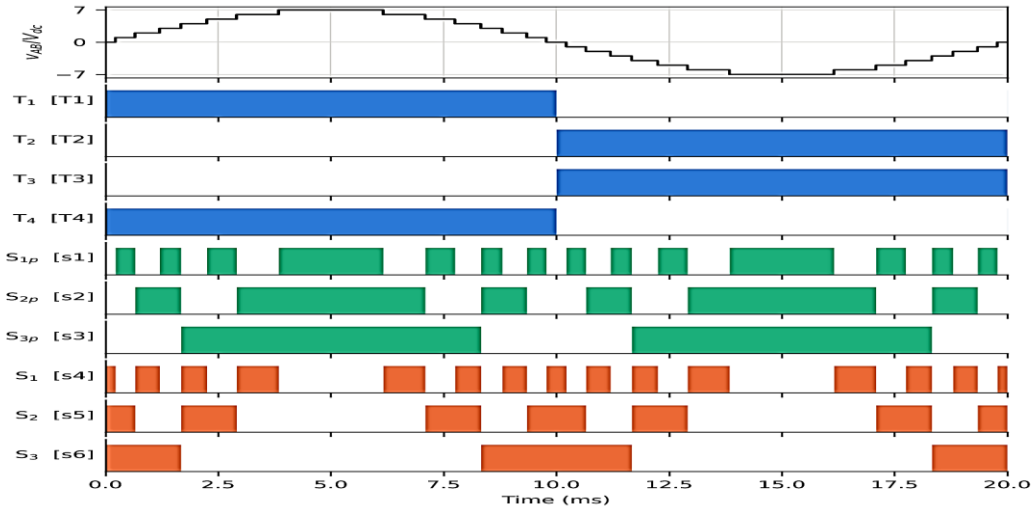

Fig. (5): Gate signals of the ten switches over one fundamental cycle for the fundamental-frequency staircase defined by the DE angles of Table 4 (switch names of Fig. 1; Simulink gate labels in brackets)

8. Simulation Results and Discussion

8.1 Optimized Switching Angles:

TABLE (4): Optimized switching angles (degrees) at M = 1.0 and analytical quality of the corresponding fundamental-frequency staircase

Quantity	DE (Modes 1, 2)	HHO (Modes 3, 4)	HHO − DE
θ_1	3.9850	4.2081	+0.2231
θ_2	11.8179	12.9537	+1.1358
θ_3	21.6353	20.7125	−0.9228
θ_4	30.1016	30.3984	+0.2968
θ_5	40.4949	40.4340	−0.0609
θ_6	52.3773	52.9070	+0.5297
θ_7	69.1235	68.6277	−0.4958
V_1 (analytical)	70.01 V	70.01 V	—
THD up to 49th (analytical)	4.62 %	4.63 %	+0.01
THD up to 1999th (analytical)	5.61 %	5.61 %	0.00

The optimized angles are compared with each other in Table 4. The optimizers ended up with nearly identical sets of angles: The maximum angle difference is 1.14° (θ_2). For a fundamental-frequency staircase, they both give a fundamental of 70.01 V, and have essentially the same distortion, namely THD 4.62% (DE) and 4.63% (HHO) up to the 49th harmonic; and THD 5.61% (DE) and 5.61%

(HHO) up to the 1999th. DE gives smaller 9th and 13th harmonics (0.15% and 0.59% vs 0.50% and 0.99%), and HHO a smaller 11th harmonic (0.49% vs 0.76%).

8.2 Output Voltage, Load Current and Spectra:

The output voltage and load current in steady state condition and their normalized harmonic spectra of both for Modes 1 and 2 (DE-PD and DE-APOD) are displayed in Figs. 6 and 7, respectively. The following spectra are presented on a full range, with the THD in the title, and on a zoomed range, where the individual harmonics are visible. The results of Modes 3 and 4 (HHO-PD and HHO-APOD) are the same as those of Modes 1 and 2 (PD and APOD), respectively, in waveforms, spectra and THD values (Table 5), and are therefore not reported again.

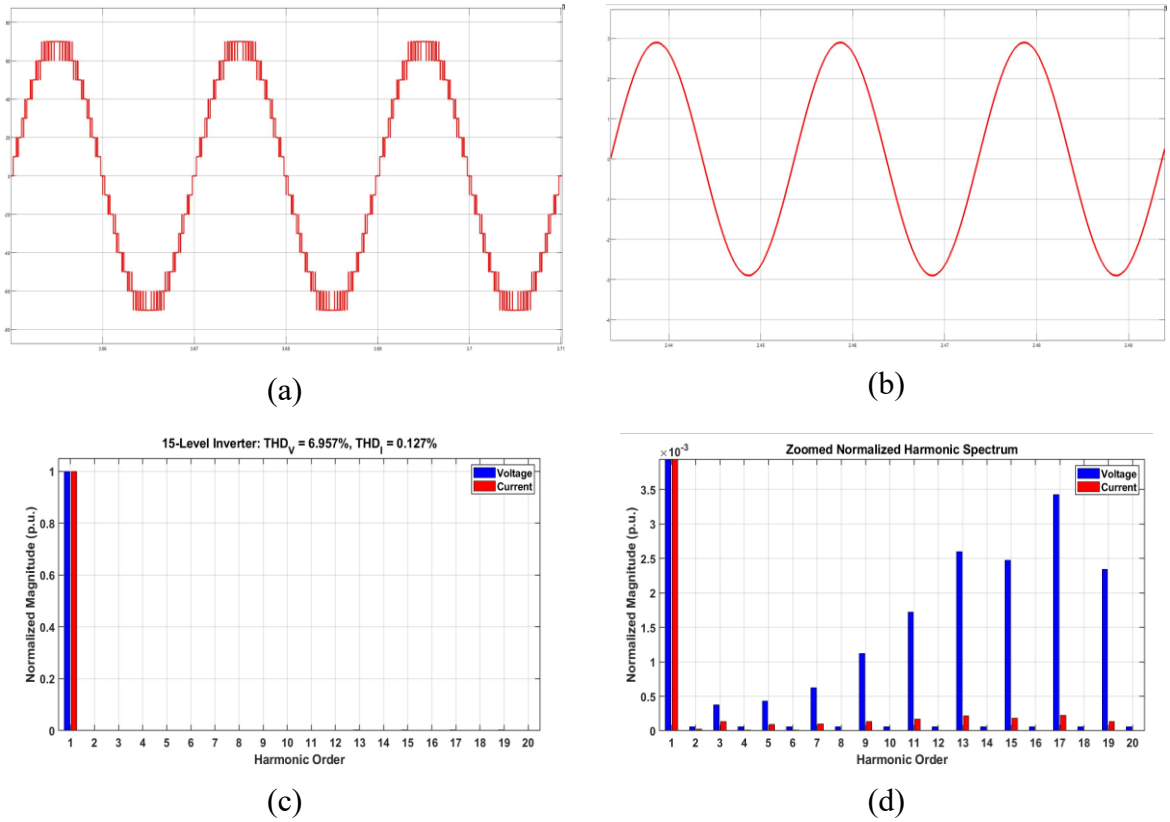

Fig. (6): Simulink results of Mode 1 (DE-PD) at M = 1.0: (a) output voltage (V) versus time (s), (b) load current (A) versus time (s), (c) normalized harmonic spectrum of voltage and current (THD_V = 6.957 %, THD_I = 0.127 %), (d) zoomed spectrum, harmonic orders 1–20. Mode 3 (HHO-PD) gave identical results

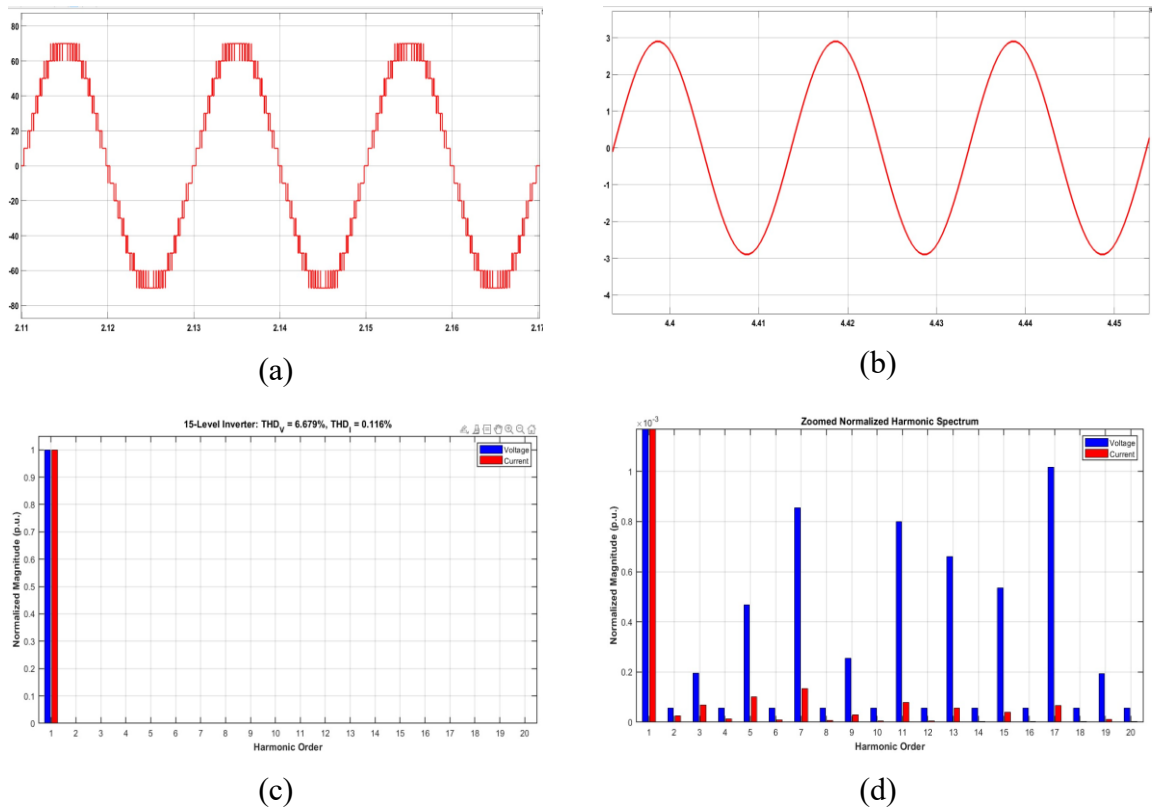

Fig. (7): Simulink results of Mode 2 (DE-APOD) at M = 1.0: (a) output voltage (V) versus time (s), (b) load current (A) versus time (s), (c) normalized harmonic spectrum of voltage and current (THD_V = 6.679 %, THD_I = 0.116 %), (d) zoomed spectrum, harmonic orders 1–20. Mode 4 (HHO-APOD) gave identical results

In all modes the resultant output voltage is a 15 level waveform with a peak voltage of 70 V ($7V_{dc}$) with the level change voltages being pulses between the levels and as predicted in Section 3. The load current is sinusoidal with a peak current of approximately 2.9 A since the higher-order harmonic currents are reduced by the inductive load.

8.3 THD and Harmonic Content:

Table (5): Simulink THD of output voltage and load current, and odd voltage harmonics (% of fundamental), at M = 1.0

Mode	THD_V (%)	THD_I (%)	h_3	h_5	h_7	h_9	h_{11}	h_{13}	h_{15}	h_{17}	h_{19}
1: DE-PD	6.957	0.127	0.04	0.04	0.06	0.11	0.17	0.26	0.25	0.34	0.23
2: DE-APOD	6.679	0.116	0.02	0.05	0.09	0.03	0.08	0.07	0.05	0.10	0.02
3: HHO-PD	6.957	0.127	0.04	0.04	0.06	0.11	0.17	0.26	0.25	0.34	0.23
4: HHO-APOD	6.679	0.116	0.02	0.05	0.09	0.03	0.08	0.07	0.05	0.10	0.02

Harmonic magnitudes are read from the zoomed spectra of Figs. 6 and 7 and are therefore approximate; even harmonics are below 0.01% in all modes.

Table 5 summarizes the distortion of the four modes. Two observations follow:

- **The Influence of the Disposition of the Carrier:** APOD's voltage THD drops from 6.957% to 6.679% (−0.278 percentage points, a 4.0% relative reduction) and the current THD drops from 0.127% to 0.116% (a 8.7% relative reduction) for both angle sets.
- **Effect of the Optimize:** Modes 1 and 3 (PD) yield the same results for THD and in the spectra, as do 2 and 4 (APOD). The DE and HHO angle sets had nearly the same angle set and had no measurable effect on the simulated output as was experienced with the DE and HHO angle sets in Section 8.1; the PWM output was determined primarily by the carrier comparison.

The 9th-19th harmonics in PD carriers increase with order of the harmonic, with the 0.26% (13th) and 0.34% (17th) harmonics being the highest values; the APOD harmonics are reduced by a factor of approximately 2–12 relative to the PD carrier values, with the 5th and 7th harmonics slightly higher. The harmonics up to 19th are about 0.59% (PD) and 0.19% (APOD) respectively when added together in a root sum square manner, and it is the load inductance that dampens such a high number of the harmonics around the carrier frequency that allows the current THD to be as low as 0.12–0.13%. To provide reference, the analytical THD of the fundamental-frequency staircase defined at the same angles is 5.61% up to the 1999th harmonic (Table 4) and a direct staircase implementation, which would also reduce the switching frequency, is a potential alternative.

9. Comparative Performance Analysis

The comparison is used to distinguish the two design options. The carrier disposition plays an important role: APOD is better than PD in voltage THD, current THD and the 9th–19th harmonics. The optimizer is not: DE and HHO were run under the same set of conditions, and the angle sets differ by no more than 1.14°, and the same Simulink results were obtained; therefore the selection between them should not be based on this criterion, but rather on a secondary criterion like computation time—consistent with the no-free-lunch theorem [28] that does not mean one is better than the other. These two types, DE-APOD and HHO-APOD, will produce the most quality output.

TABLE (6): Comparison with related published studies (qualitative; THD values depend on the number of levels, phase configuration, harmonic range and modulation index)

Study	Levels	Switches	DC sources	Modulation / angle computation	Reported output quality
This work	15	10	3 (1:2:4)	DE / HHO angles with PD and APOD LS-PWM	THD_V = 6.679 %, THD_I = 0.116 % (APOD, M = 1.0, sim.)
Fahad et al. 2021 [17]	15	12	4	Nearest-level control	see source
Bin Arif et al. 2021 [18]	15	10	4	Nearest-level control	see source
Orfi Yeganeh et al. 2021 [20]	15 / 25	reduced	multiple	PSO optimal angles	see source (prototype)
Kumar et al. 2024 [27]	9	—	—	HHO vs PSO, ACO (SHE)	5.34 % sim., 5.97 % exp. (M = 0.85)
Ahsan et al. 2023 [25]	7 (CHB)	12	3	Broyden-assisted DE	eliminates 3rd, 5th

In comparison to the four-source 15-level topologies like [17] and [18] (Table 6) the studied circuit

requires just one less source and two fewer switches than [17], albeit with increased TSV due to the H-bridge. IEEE Std 519 only applies its distortion limits at the point of common coupling of an installation and not to the terminal voltage of a single converter [30]; the THD values reported here characterize the inverter waveform and do not necessarily establish compliance.

10. Conclusion

For M = 1.0, four operating modes of a ten-switch 15-level asymmetric multilevel inverter with binary DC sources 10 V, 20 V and 40 V were analysed and simulated using MATLAB/Simulink. All 1024 switching combinations were tested and it was found that there are 15 output levels, 1 switching state for each of the non-zero output levels with a total standing voltage of $42V_{dc}$. Under identical conditions DE and HHO yield angle sets that differ by at most 1.14° with virtually the same analytical quality, THD of 4.62 % and 4.63 % respectively. The voltage THD was reduced by 4.0%, the current THD by 8.7% and the 9th–19th harmonics by a factor of approximately 2–12 with APOD, while these were not measurably affected by optimization choice; with the voltage THD of 6.957% and the current THD of 0.127% for both PD modes and 6.679% and 0.116% for both APOD modes, respectively. Therefore, among the four modes studied, the APOD ones are recommended.

The results are all simulated with ideal DC sources and no experimental validation is claimed. Future work will consist of an actual fundamental-frequency staircase implementation of the optimized angles, evaluation of the entire modulation range, source-voltage deviations, and device losses and dead time, and hardware testing.

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