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# Resilient Waveform Employing FPGA Configuration

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## Abstract

Since the high-bit loading concept has attracted the attention of the wireless communication community, an important level of processing, like the digital modulation process, should be exploited efficiently. Thus, due to the challenging requirements of future mobile networks, particularly those related to big-data applications, the huge channel capacity of wireless communication represents a significant topic for the upcoming mobile technology. In this paper, the impact of utilizing the field programmable gate array (FPGA) for the developed waveform shape of the fifth generation (5G) mobile and beyond is demonstrated. The performance of transmission in terms of improved bit-rate is smoothly processed under the FPGA domination and in an electrical back-to-back wireless network system. By employing the elastic features of the FPGA, the advanced modulation formats are introduced herein as an effective solution for the physical layer (PHY) of the transmission system. As such, getting a higher bandwidth (BW) efficiency is softly obtained by adopting a flexible manipulation for the enhanced bit loading technique. Thus, in contrast to the conventional application- specific integrated circuit (ASIC) that is struggling to deal with an updated shape of modulation unless changing the whole infrastructure, the resilient platform of the FPGA can enhance the modulation process while keeping the existing hardware design. Therefore, by updating the installed software of the FPGA, the modulation level can be easily promoted from the low-level to the high-level modulation schemes.

**Keywords:** Field Programmable Gate Array (FPGA), Application- Specific Integrated Circuit (ASIC), Wireless Mobile Networks.

## Introduction

As a vital driving force for the fast-growing wireless mobile networks, the system performance of the future communication system, mainly for high-data transmission, has been highly considered recently [1]. Thus, since the high bit-rate becomes an imperative necessary for the next mobile technology, the modulation formats, mostly, the higher shapes of them can be accounted as one of the best options used for this purpose. Hence, by utilizing an extra bit loading, a better bandwidth (BW) efficiency can be obtained [2]. In this context, the traditional way from a hardware (HW) viewpoint is utilising the application-specific integrated circuit (ASIC) for getting new designs with updated abilities of wireless transceiver systems [3]. Nevertheless, the physical approach faced mainly a critical problem related to expansion limitation, resulting in a totally changed system whenever development is

intended [4]. This comes up with fully replacing HW and Software (SW) tools for enlarging transmission rate, especially transferring from low to higher modulation formats [5].

To address this problem, a resilient solution is presented herein at the physical layer, yielding a new wireless transceiver model with additional variation capability. Accordingly, the field programmable gate array (FPGA) is proposed herein to digitally achieve a new flexible design of the orthogonal generalized frequency division multiplexing (OGFDM). Hence, utilizing the FPGA platform, a modulation level with a scalable process is fundamentally obtained. Therefore, depending on the FPGA approach, the same construction blocks of the H/W device are reused by updating just the S/W programming [6].

By combining the FPGA platform with the digital signal processing (DSP) component of the waveform technology, the developers of wireless waveforms can smoothly perform their prototype designs, relying on the reprogrammable domain. Thus, the required modulation style is not tied to a specific integrated circuit (IC) purpose, as is the ASIC. As such, without replacing the silicon chip, the needed modulation layout is easily transferred and applied to the electrical piece [7].

Considering the changeable criterion of the portable code, the implemented modulation can be applied while keeping the main IC structure without any change. Consequently, the adaptable system based on an FPGA makes alternating to varied types of modulation formats entirely possible. As such, the free FPGA stage, unlike the restricted-chip ASIC, can be continuously reconfigured even following processing, in accordance with changing H/W functionality [8].

Worth mentioning that, FPGA manipulation comes up with an independent level of processing, which basically picks the intended modulation scheme regardless of the word width size. The proposed handling of FPGA can supply a cooperative environment between the temporarily applied S/W and the permanently existing H/W. Moreover, employing a developed hardware programming like the very high-speed description language (VHDL), an efficient modelling and simulation for applied digital systems (FPGA) is achieved [9].

The significant advantages of utilizing the FPGA, in comparison to the traditional ASIC, are summarized as follows:

1. Flexibility: Instead of being replaced as the ASIC does, the IC-based FPGA can be reconfigured repetitively according to the demanded application by utilising the FPGA programmable feature. Hence, a high level of flexibility can be obtained with an FPGA relative to the limited design of an ASIC circuit [10].

2. Expandability: To cope with the new functional necessities of wireless transmission, sometimes, portions of the digital system need to be improved, extended, or even changed. To accomplish this, upgrading the installed FPGA code can be easily achieved without entirely replacing the H/W [11].

3. Simplicity: As the key part of the resilient waveform-based FPGA performs digitally, the central controller of the adapted transceiver slightly requests peripheral devices. Thus, the embedded

processing of the FPGA looks only for the sampling converters where the signal is converted between the digital and analogue domains, making the proposed design concise and simple. Nevertheless, the digital system that relies on the FPGA requested higher power consumption than the comparative ASIC [12].

Worth noting that the applied waveform, which is highly recommended for the upcoming wireless networks [13], has also been developed to work in the optical domain [14]; nonetheless, the proposed solution can be compatible with both cases (electrical/optical) since the concepts of the modulation stage are still similar regardless of the waveform domain.

This paper is organized as follows: In Section II, the system model is presented for the proposed modulation process. Section III is dedicated to the experimental field using the FPGA handling. Finally, section IV is the paper's conclusion.

## System Model

In this presented model, a highly flexible design of wireless communication with an extra transmission bit rate and a low cost is introduced. Therefore, utilizing the FPGA instead of the ASIC for executing the digital processing of the signal results in an elastic physical layer of the waveform.

As is seen in Fig. 1, on the transmitter side of the waveform environment, the FPGA platform is essentially assigned for the digital domain. Accordingly, in the modulation level, which represents the starting stage, the required complex numbers are generated by directly changing every corresponding single token of the binary stream with the chunk size (X) bits. The capability to transport an additional number of bits is improved in accordance with the increased size of the chunk. Thus, for each promoted level of modulation layout, a high degree of transmission rate is realized.

Worthy that by applying the proposed solution based on the FPGA, the system just needs to upgrade the S/W coding without changing the infrastructure (H/W) of the transceiver. Consequently, to support higher modulation types like the 128 or 265 Quadrature Amplitude Modulation (QAM), the system can perform this by a simple and elastic adaptation, in contrast to the complicated and fixed design-based ASIC. This results in efficiently lifting the bit-rates of the transmission by reducing the cost of updated modulation expansion. Since both frequency and time domains already exist in the digital mode, the signal is transferred to the time domain, passing through the oversampling and filtration process. After that, at the end of the digital handling, to supply an extra level of protection, the entire block of waveform symbols is potentially accompanied by guard intervals, which are commonly known as a cyclic prefix (CP). Eventually, the digital signal leaves the DSP-based FPGA part for the main peripheral digital-to-analogue converter (DAC) to transform to the analogue domain. Later, the analogue signal is communicated through the wireless back-to-back system using a suitable antenna.

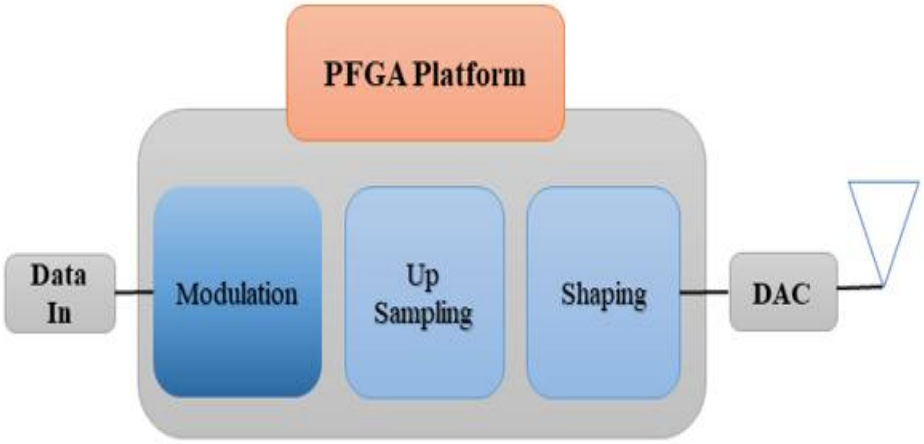


Fig. 1.Flexible transmitter based on the FPGA platform.

As in Fig. 2, on the receiver side, a reverse processing is performed where an external peripheral device analogue to digital converter (ADC) transforms the signal to the digital domain to be ready for the FPGA system. Then, at the FPGA, for every two adjacent symbols of the waveform, the CP that was added previously is removed. After, the signal is resumed in the frequency domain in a reversal procedure. Finally, the stream of binary digits is recovered from the received complex numbers at the demodulation side. Worthy, any possible update at the modulation level is synchronically applied on the other side (demodulation level), ensuring compatibility during the transmission operation. Thus, if the modulation operation starts, for example, with 16 QAM, then moves to 64 QAM, and ends with 256 QAM, the demodulation will be handled accordingly by converting to 16 QAM, 64 QAM, and 256 QAM, respectively. Therefore, changing bit loading for each subcarrier is smoothly performed at the modulation, and can be easily recognized and recovered at the demodulation. This, as such, gives the proposed system the flexibility in transferring the modulation from one format to another because of the nature of programmable HW of the FPGA.

Mathematically speaking, in Cartesian form, mainly, in the modulation process of the transmitter, each picked portion of the binary stream digits is transformed to a corresponding complex number ($N_c$) as follows: [15]

$$N_c = R_c + I_c f \ldots\ldots\ldots\ldots (1)$$

where $f=\sqrt{-1}$, and for the *cth* sample, $R_c$, $I_c$ refer to the real and imaginary parts, respectively.

Accordingly, the magnitude (M) of each frequency is generated based on the gained complex number as follows: [15]

$M_c = \sqrt{(R_c + I_c)}$ …… (2)

Besides, the frequency phase (Θ) is produced by a complex number as follows: [15]

$\Theta_c = \tan^{-1} = I_c / R_c$ …... (3)

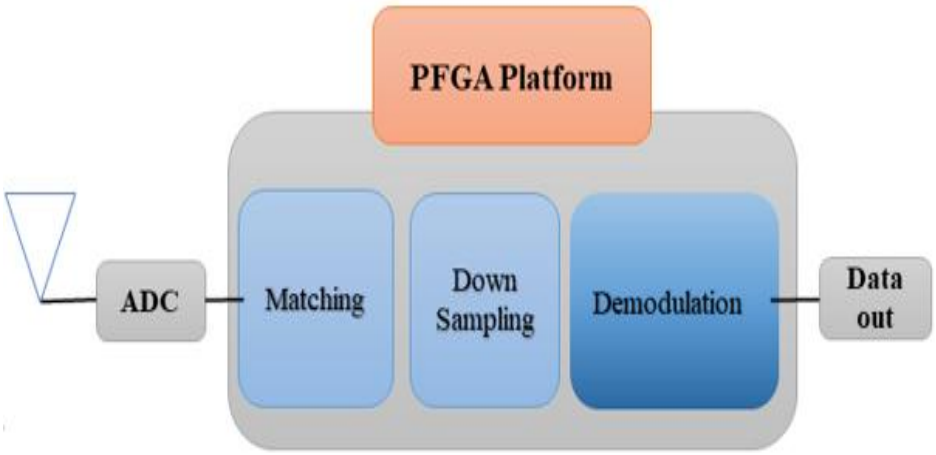


Fig. 2. Flexible receiver based on the FPGA platform.

## Experimental Work

In this part, the 5CSEMA5F31C6N-FPGA device is experimentally used to demonstrate the key features of employing the FPGA platform with the applied waveform system, thereby enabling an elastic, easy, and low-cost elevation of the modulation process. Four key scenarios are explored for the modulation part of the developed waveform to investigate the influence of exploiting the platform 5CSEMA5F31C6N-FPGA on the initial components of the digital signal processing unit. Accordingly, in this experiment, to handle variant levels of bit loading, low, medium, high, and advanced, 4 QAM, 16 QAM, 64 QAM, and 256 QAM are represented, respectively. Therefore, by considering these studied scenarios, the tested system can smoothly describe the correlation between the infrastructure of the embedded modulation format and the FPGA platform. This, as such, comes up with presenting, via the experiment, the key advantages of employing the FPGA technology for the advanced waveform.

In Fig. 3, the first scenario (low modulation), which is related to 4 QAM, is shown. Thus, since every two bits need to be converted to their corresponding single complex number, two input lines that represent the word size are employed for introducing the intended complex number. In this context, as an example, the complex number $1 - 1f$, where $f = \sqrt{-1}$, is generated by setting the input token of two bits to 10.

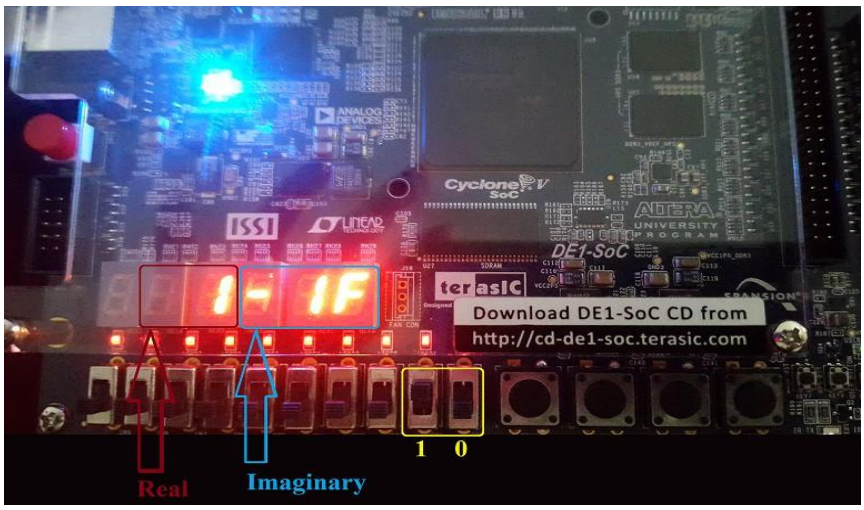


Fig. 3. 4QAM modulation over the FPGA platform.

A snapshot of VHDL code that describes the implementation of the structural design of the 4 QAM on the FPGA board is shown in Fig. 4.

```
 5   LIBRARY ieee;
 6   USE ieee.std_logic_1164.all;
 7   ENTITY QPSK IS
 8   PORT (
 9   SW : IN STD_LOGIC_VECTOR(9 DOWNTO 0);
10   HEX0: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
11   HEX1: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
12   HEX2: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
13   HEX3: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
14   HEX4: OUT STD_LOGIC_VECTOR(6 DOWNTO 0)
15   );
16   END QPSK;
17
18   ARCHITECTURE Behavior OF QPSK IS
19
20   component  C_to_7Seg is
21       port(
22               c: in std_logic_vector(1 downto 0);
23               Hx: out std_logic_vector(6 downto 0)
24              );
25
26   end component;
27   component shifting is
28       port(
29               c: in std_logic_vector(1 downto 0);
30               SH: out std_logic_vector(9 downto 0)
31              );
32
33   end component;
34   signal temp :STD_logic_vector(9 downto 0);
35   BEGIN
36
37           shift: shifting port map(SW(1 downto 0),temp);
38           dd: C_to_7Seg port map(temp(1 downto 0),HEX0);
39           ee: C_to_7Seg port map(temp(3 downto 2),HEX1);
40           rr: C_to_7Seg port map(temp(5 downto 4),HEX2);
41           kk: C_to_7Seg port map(temp(7 downto 6),HEX3);
42           mm:C_to_7Seg port map(temp(9 downto 8),HEX4);
43   END Behavior;
```

Fig. 4. VHDL code of 4QAM implemented on the FPGA board.

In Fig. 5, the second scenario (16 QAM), which represents the medium modulation level, is declared. Accordingly, 4 bits (token size) are specified to represent every point at constellations table. Therefore, by moving to higher bit loading and assigning, for instance, 1010 as an input value for the

four device lines, the resulting complex number after processing is 3 − 3f. Consequently, expanding the probability of the points at the Gray map to $2^4$ rather than $2^2$ of the first one.

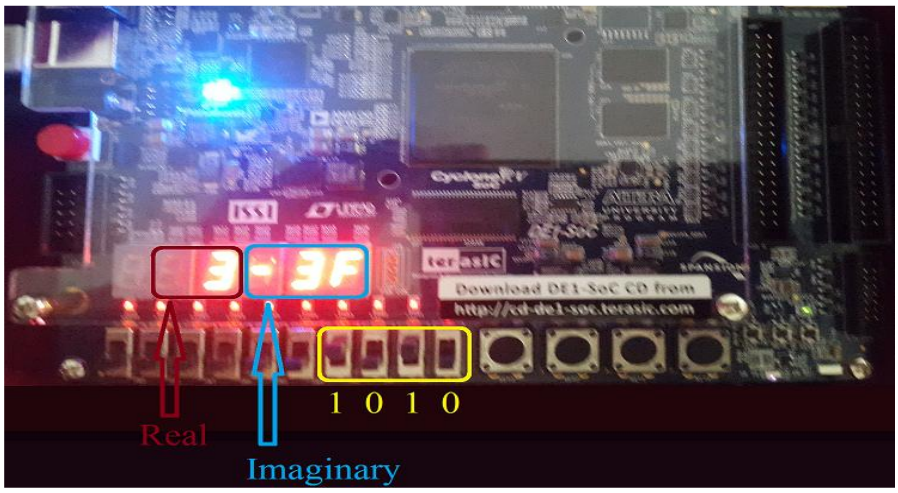


Fig. 5. 16 QAM modulation over the FPGA platform.

The VHDL code that demonstrates the structural design implementation of the 16 QAM on the FPGA board is shown in Fig.6.

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY QAM16 IS
PORT (
SW : IN STD_LOGIC_VECTOR(9 DOWNTO 0);
HEX0: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
HEX1: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
HEX2: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
HEX3: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
HEX4: OUT STD_LOGIC_VECTOR(6 DOWNTO 0)
);
END QAM16;

ARCHITECTURE Behavior OF QAM16 IS

component  C_to_7Seg is
    port(
            c: in std_logic_vector(2 downto 0);
           Hx: out std_logic_vector(6 downto 0)
          );

end component;
component shifting is
    port(
            c: in std_logic_vector(3 downto 0);
           SH: out std_logic_vector(14 downto 0)
          );

end component;
signal temp :STD_logic_vector(14 downto 0);
BEGIN

       shift: shifting port map(SW(3 downto 0),temp);
       dd: C_to_7Seg port map(temp(2 downto 0),HEX0);
       ee: C_to_7Seg port map(temp(5 downto 3),HEX1);
       rr: C_to_7Seg port map(temp(8 downto 6),HEX2);
       kk: C_to_7Seg port map(temp(11 downto 9),HEX3);
       XX: C_to_7Seg port map(temp(14 downto 12),HEX4);

END Behavior;
```

Fig. 6. VHDL code of 16 QAM implemented on the FPGA board.

In Fig. 7, as moving to the high level of modulation requires further allocation of bits, a word size of 6 bits is used herein. Thus, to represent the expected complex numbers of the 64 QAM modulation, 6 lines are reserved to introduce the corresponding value in the frequency domain. Subsequently, at

the constellation table of the 64 QAM, the complex number 1−5f is obtained by setting the token lines to 110001.

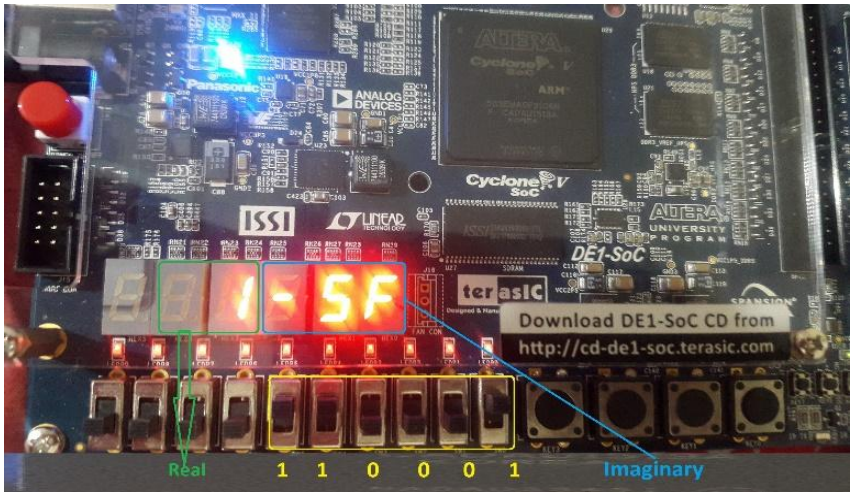


Fig. 7. 64 QAM modulation over the FPGA platform.

The VHDL code on the FPGA board for implementing the structural design of the 16 QAM is seen in Fig.8.

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY QAM64 IS
PORT (
SW : IN STD_LOGIC_VECTOR(9 DOWNTO 0);
HEX0: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
HEX1: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
HEX2: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
HEX3: OUT STD_LOGIC_VECTOR(6 DOWNTO 0) ;
HEX4: OUT STD_LOGIC_VECTOR(6 DOWNTO 0)
);
END QAM64;

ARCHITECTURE Behavior OF QAM64 IS

component  C_to_7Seg is
    port(
            c: in std_logic_vector(2 downto 0);
            Hx: out std_logic_vector(6 downto 0)
           );

end component;
component shifting is
    port(
            c: in std_logic_vector(5 downto 0);
            SH: out std_logic_vector(14 downto 0)
           );

end component;
signal temp :STD_logic_vector(14 downto 0);
BEGIN

        shift: shifting port map(SW(5 downto 0),temp);
        dd: C_to_7Seg port map(temp(2 downto 0),HEX0);
        ee: C_to_7Seg port map(temp(5 downto 3),HEX1);
        rr: C_to_7Seg port map(temp(8 downto 6),HEX2);
        kk: C_to_7Seg port map(temp(11 downto 9),HEX3);
        XX: C_to_7Seg port map(temp(14 downto 12),HEX4);
END Behavior;
```

Fig. 8. VHDL code of 64 QAM implemented on the FPGA board.

In Fig. 9, as it is clear, the fourth scenario indicates the advanced modulation format (256 QAM), where 8 bits' worth of data maps to 8 input lines to accommodate each complex number. In this developed case, which extremely increases BW efficiency and transmission bit-rate, supplying extra lines (8), for example, with 11010000, produces a complex number equivalent to 9 − 7f.

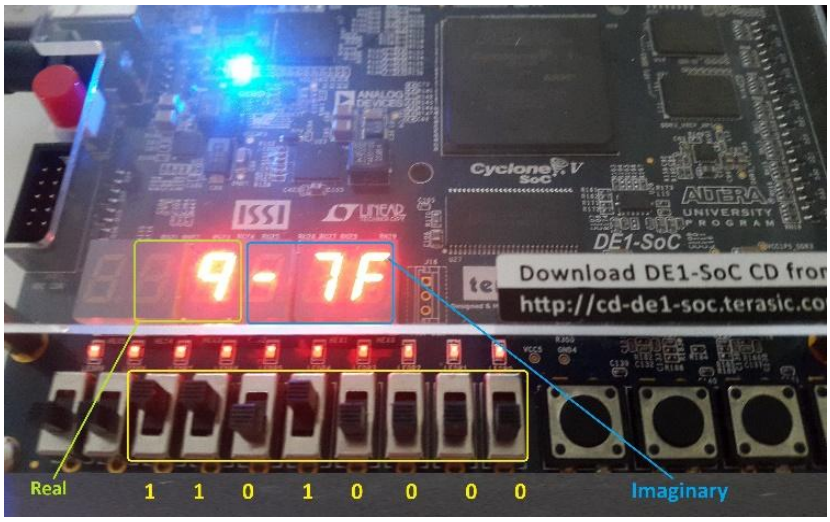


Fig. 9. 256 QAM modulation over the FPGA platform.

The VHDL code for describing the implemented design of the 256 QAM on the FPGA board appears in Fig. 10.

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY QAM256 IS
PORT (
SW : IN STD_LOGIC_VECTOR(9 DOWNTO 0);
HEX0: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
HEX1: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
HEX2: OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
HEX3,HEX4: OUT STD_LOGIC_VECTOR(6 DOWNTO 0)
);
END QAM256;

ARCHITECTURE Behavior OF QAM256 IS

component  C_to_7Seg is
    port(
           c: in std_logic_vector(2 downto 0);
          Hx: out std_logic_vector(6 downto 0)
         );

end component;
component shifting is
    port(
           c: in std_logic_vector(7 downto 0);
          SH: out std_logic_vector(14 downto 0)
         );

end component;
signal temp :STD_logic_vector(14 downto 0);
BEGIN

      shift: shifting port map(SW(7 downto 0),temp);
      dd: C_to_7Seg port map(temp(2 downto 0),HEX0);
      ee: C_to_7Seg port map(temp(5 downto 3),HEX1);
      rr: C_to_7Seg port map(temp(8 downto 6),HEX2);
      kk: C_to_7Seg port map(temp(11 downto 9),HEX3);
      XX: C_to_7Seg port map(temp(14 downto 12),HEX4);
END Behavior;
```

Fig. 10. 256 QAM modulation over the FPGA platform.

Based on the explored scenarios, it's worth mentioning that even though varying the applied modulation schemes, the H/W based on the FPGA platform is still valid. Therefore, contrasting the conventional ASIC, variant modulation formats required different S/W adaptations without any change for the H/W. Accordingly, employing the flexible environment, the modulation system easily developed its bit loadings from the lower to the upper, in contrast with the traditional ASIC.

As in Fig. 11, according to Shannon theory, the capacity of the applied channel BW is enlarged mainly by maximizing the bits transmitted over. Such, by comparing the obtained transmission capacities of the presented modulation formats, starting with 4 QAM, to 16 QAM, 64 QAM, and ending with 256 QAM, varied levels of BW efficiency are recorded. Thus, via expanding the assigned bit loading from two bits (4 QAM) to 8 bits (256 QAM), the measured efficiency is highly increased in the offered BW. For this reason, improving the performance of the transmission system in terms of the obtained channel capacity is directly related to promoting the utilized modulation format.

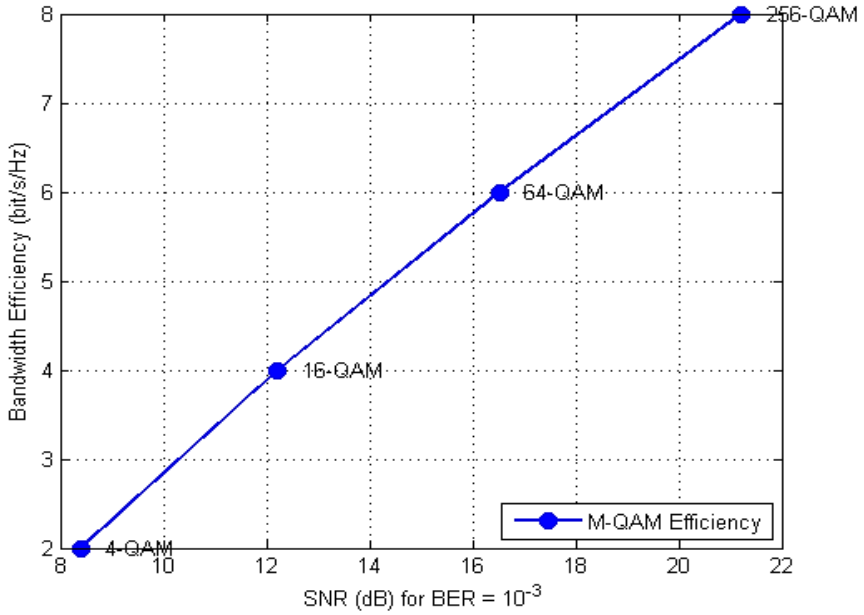


Fig. 11. Improved channel capacity with higher modulation.

The system performance in terms of the required signal-to-noise ratio (SNR) and recognized BER should be considered. Hence, by moving to a higher modulation format, the needed SNR is raised. Accordingly, as the bit loading increases, the consumed power grows. The main reason is that the high modulation shape requires extra power to ensure sample recognition on the constellation map. Thus, unless elevating the SNR, the transmitted signal with improved modulation is not being received correctly.

## Conclusion

In this paper, the FPGA platform is utilized to achieve an elastic, efficient, and enhanced manipulation for the modulation format of the advanced 5G mobile waveform. The presented system provides a smooth transition to a higher transmission bit rate, effective and cost-effective sharing of PHY resources, and low-cost installation of an electrical back-to-back wireless network. Relative to the traditional ASIC, the digital modulation process based on the FPGA is easily updated, resulting in a flexible adaptation of the waveform bit loading system. From an experimental perspective, the programmability of FPGAs comes into play by reconfiguring the employed IC to match the requested modulation scheme. Therefore, instead of replacing the IC whenever need for traditional modulation, the proposed design tends to deploy the SW handling to obtain a more expandable, simple, and flexible modulation system. The resilient design of the FPGA enables moving efficiently among different formats of modulation, such as the 4QAM, 16QAM, 64QAM, and 256QAM, overcoming the design limitation of the ASIC. To meet the future communication functionalities that relate particularly to the increased bit rate of heterogeneous networks, it's highly recommended to consider the FPGA for effective modulation, keeping the applied H/W without changes. Besides, apart from the extra power consumption of the FPGA, the introduced solution can maximize channel bit rate economically since replacing only the S/W is quite cheaper than exchanging both the S/W and the H/W.

## References

[1] M. Agiwal, A. Roy, and N. Saxena,"Next Generation 5G Wireless Networks: A Comprehensive Survey," IEEE Commun. Surv. Tutorials, vol. 18, no. 3, pp. 16171655, 2016.

[2] G. Liu and D. Jiang, "5G: Vision and Requirements for Mobile Communication System towards Year 2020," Chinese J. Eng., vol. 2016, no. March, 2016.

[3] A. Amara, F. Amiel, and T. Ea,"FPGA vs. ASIC for low power applications,", Microelectronics J., vol. 37, no. 8, pp. 669677, 2006.

[4] M. S. Abdelfattah and V. Betz, "Design tradeoffs for hard and soft FPGA-based networks-on-chip,", FPT 2012 - 2012 Int. Conf. FieldProgrammable Technol., pp. 95103, 2012.

[5] Y. Zhuan, J. Grosspietsch, and G. Memik, "An FPGA based all-digital transmitter with radio frequency output for software defined radio,", Proc. -Design, Autom. Test Eur. DATE, pp. 2126, 2007.

[6] J. McCollum, "ASIC versus antifuse FPGA reliability,", IEEE Aerosp. Conf. Proc., pp. 111, 2009.

[7] M. Salah, A. H. Zekry, and M. Kamel,"An efficient FPGA implementation of OFDM physical layer for SDR-based applications,", 2014 10th Int. Comput. Eng. Conf. Today Inf. Soc. Whats Next?, ICENCO 2014, pp. 145148, 2015.

[8] F. Abid and N. Izeboudjen,"Technology-independent approach for FPGA and ASIC implementations,", 2015 4th Int. Conf. Electr. Eng. ICEE 2015, pp. 14, 2016. doi: 10.1109/CECNET.2011.5768218.

[9] G. M. Sung, H. K. Wang, and J. H. Lin,"Serial interface engine ASIC with USB physical transceiver based on FPGA development board,", 2017 IEEE Int. Conf. Syst. Man, Cybern. SMC 2017, vol. 2017Janua, pp. 410413, 2017.

[10] M. Zhang and H. Zhang, "Design and implementation of wireless transceiver system based on FPGA,", CICC-ITOE 2010 - 2010 Int. Conf. Innov. Comput. Commun. 2010 Asia-Pacific Conf. Inf. Technol. Ocean Eng., pp. 355357, 2010.

[11] T. Sato, S. Chivapreecha, P. Moungnoul, and K. Higuchi,"An FPGA architecture for ASIC-FPGA co-design to streamline processing of IDSs," Proc. - 2016 Int. Conf. Collab. Technol. Syst. CTS 2016, pp. 412417, 2016.

[12] Y. Liu et al., "Waveform Candidates for 5G Networks: Analysis and Comparison,", ArXiv, pp. 117, 2016.

[13] M. R. Kadhum, ''Upgrading physical layer of multi-carrier OGFDM waveform for improving wireless channel capacity of 5G mobile networks and beyond,'' Information, vol. 11, no. 1, p. 35, Jan. 2020

[14] M. R. Kadhum and H. Haboobi, "Advanced Optical Waveform With Single Mode Fiber Optic for Developing Upcoming Networks of Mobile Communications," in IEEE Access, vol. 13, pp. 6413-6421, 2025.

[15] H. Haboobi and M. R, Kadhum ''Impact study and evaluation of higher modulation schemes on physical layer of upcoming wireless mobile networks,'' Int. J. Adv. Comput. Sci. Appl., vol. 10, no. 5, pp. 665–676, 2019.